UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/681,445	10/08/2003	Sung Mao Wu	4459-134	7120

22429 7590 04/21/2005

LOWE HAUPTMAN GILMAN AND BERNER, LLP
1700 DIAGONAL ROAD
SUITE 300 /310
ALEXANDRIA, VA 22314

EXAMINER	
PAREKH, NITIN	

ART UNIT	PAPER NUMBER
2811	

DATE MAILED: 04/21/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/681,445	WU ET AL.	
	Examiner	Art Unit	
	Nitin Parekh	2811	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *01 April 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *2-21* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *2-21* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *29 October 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Based on applicant's arguments dated 04-01-05, the finality of the previous Office action is hereby withdrawn pursuant to 37 CFR 1.129(a).

2. Applicant's amendment after final filed on 04-01-05 has been entered.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 2-5, 7-15 and 17-21 are rejected under 35 U.S.C. 103(a) as being unpatentable over Newman (US Pat. 5490324) in view of Brooks et al. (US Pat. 6084297).

Regarding claims 2-5 and 7-10, Newman discloses a ball grid array (BGA) package (see Fig. 6) comprising:

- a composite substrate (CS-504/506/508 in Fig. 6) having an upper surface and a lower surface, the substrate comprising:
    - o a first laminated layer comprising printed wiring board (PWB) layers including internal conductive/circuit patterns (see 506/508 in Fig. 6)

- a second PWB layer/insulating layer positioned below the first layer (see 504 in Fig. 6), the PWB layers being reinforcement-containing insulating layers and being formed from conventional glass-reinforced epoxy/FR4/insulating material (Col. 1, line 40)
- a recessed cavity (520/522 in Fig. 6) defined in the upper surface of the CS and in the first laminated layer,
- a plurality of chip contact pads (514 in Fig. 6) formed on the surface of the reinforcement-containing insulating layer/second PWB layer and exposed from the recessed cavity
- a plurality of solder ball terminals/pads (see 510 connected to respective conductive sites in Fig. 6) formed on conductive/circuit patterns (see 524 in Fig. 6) on the upper surface of the CS and outside the recessed cavity for making external electrical connections
- the chip contact pads being electrically connected to the solder ball terminals/pads through respective wiring/internal circuit patterns/traces including those on the upper surface of the reinforcement-containing insulating layer/second PWB layer (see 602/604 in Fig. 6)

- a semiconductor die/chip (502 in Fig. 6) disposed in the recessed cavity of the substrate and mechanically/electrically interconnected to the chip contact pads via bonding wires (610a/610b in Fig. 6)

- the BGA package comprising a metal layer/heat conducting layer/metal coating formed on the lower/bottom surface of the substrate defining an outermost bottom surface of the package (see 620 in Fig. 6), and
- a plurality of conductive vias (see Fig. 6) formed through the PWB layers including those extending entirely through the second PWB layer/reinforcement-containing insulating layer (see 616 in Fig. 6) to connect respective wiring/circuit patterns/traces on the surface of the second PWB (see 616 connecting 514/602, 524/upper conductive pattern and 620/bottom conductive layer in Fig. 6; Col. 9, line 35- Col. 10, line 20) with top and bottom conductive layers to provide an electrical path from the chip through the respective conductive vias to the respective solder ball terminals/pads, the metal layer/coating and to an outside of the package (Col. 9, lines 35-Col. 10, line 11), and

- an encpasulant/molding compound/epoxy resin (614 in Fig. 6) formed in the cavity between the semiconductor chip and substrate

(Fig. 6; Col. 9, line 10- Col. 10, line 20; Col. 1-7 and 9-11).

Newman fails to teach the BGA package being a flip chip configuration by having the chip connected by flip chip bonding such that the conductive vias electrically connect the metal coating and the chip contact pads.

Brooks et al. teach BGA packages having a cavity and a chip connected to an insulating substrate (see 14 and 16 respectively in Fig. 2/5) wherein the substrate comprises conventional metallization on upper and lower surfaces including connecting sites/pads/traces (see 22/44 and 20/24 respectively in Fig. 2) and a plurality of electrically conductive vias (see 34 in Fig. 2) through the substrate such that the vias provide the desired electrical connection between the chip pads and the metallization on the upper/lower surfaces (see Col. 5). Furthermore, Brooks et al. the BGA having conventional configurations such as wire bonding or flip chip bonding (see Fig. 2 and 5 respectively) wherein the flip chip configuration (Fig. 5; Col. 8; Col. 5-8) comprises:

- the chip being mechanically/electrically interconnected to the chip contact pads via solder joints/bumps (see 126/46 in Fig.5)
- a heat sink disposed on the top of the chip (see 50/51 in Fig. 5) to provide a thermal path for heat dissipation, and
- the cavity being filled with conventional encapsulant/epoxy/underfill between the chip and the substrate/insulating layer (not numerically referenced in Fig. 5; see Col. 7, lines 10-25).

It would have been obvious to a person of ordinary skill in the art at the time invention was made to incorporate the flip chip configuration by having the chip connected by flip chip bonding the conductive vias electrically connect the metal coating and the chip contact pads as taught by Brooks et al. so that the desired electrical and

thermal performance can be achieved, connection density and reliability can be improved and the package dimensions can be reduced in Newman's package.

Regarding claims 11-15 and 17-21, Newman and Brooks et al. teach substantially the entire structure as applied to claims 2-5 and 7-10 above.

5. Claims 6 and 16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Newman (US Pat. 5490324) and Brooks et al. (US Pat. 6084297) as applied to claims 4 and 11 above, and further in view of Marrs et al. (US Pat. 5583378).

Regarding claims 6 and 16, Newman and Brooks et al. teach substantially the entire structure as applied to claims 4 and 11 respectively above, except the reinforcement-containing insulating layer/insulating layer being made of BT (bismaleimide-triazine) resin.

Marrs et al. teach a flip chip package comprising an insulating layer of PWB substrate being made of conventional BT resin (see Col. 8, line 33).

It would have been obvious to a person of ordinary skill in the art at the time invention was made to incorporate the reinforcement-containing insulating layer/insulating layer being made of BT resin as taught by Marrs et al. so that rigidity and the insulating properties of the substrate can be improve in Newman's package.

Response to Arguments

6. Applicant's arguments filed on 04-01-05 have been fully considered but they are not persuasive.

A. Applicant contends that the thermal vias in Newman's BGA do not electrically connect the metal coating and the chip pads.

However, as explained above, the conductive vias (see 616 in Fig. 6) formed through the second PWB layer/reinforcement-containing insulating layer connect respective wiring/circuit patterns/traces (see 616 connecting 514/602 and 620/bottom conductive layer in Fig. 6; Col. 9, line 35- Col. 10, line 20) with top and bottom conductive layers to provide the electrical connection from the chip to the respective solder ball terminals/pads, the metal layer/coating and to the outside of the package.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Nitin Parekh whose telephone number is 571-272-1663. The examiner can normally be reached on 09:00AM-05:30PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Lee can be reached on 571-272-1732. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9318.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-0956.

NP

04-13-05

NITIN PAREKH

PRIMARY EXAMINER

TECHNOLOGY CENTER 2800